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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,641	12/08/2003	Paul A. Farrar	1303.041US2	2954

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,641	FARRAR, PAUL A.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-14,16-18,20-22,24-27,29-32 and 34-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14,16-18,20-22,24-27,29-32 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 20, 21 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (U.S. Patent No. 6,268,637 B1) in view of Delgado et al. (U.S. Patent No. 5,949,144).

In re claims 1, 20 and 24, Gardner discloses a semiconductor device, comprising:

A substrate (12) including:

a dielectric layer (SOI substrate ; column 3, lines 50-51)

a semiconductor layer formed over the substrate;

a first active region (22) formed in the semiconductor layer;

a second active region (24) formed in the semiconductor layer;

a trench (26) formed in the substrate and interposed between the first active region and the second active region; and

wherein the trench contains cells of gaseous components within an air gap (column 6, lines 16-18).

Gardner does not expressly disclose the SOI substrate including an air gap for location at least partially beneath the active region. Delgado (esp. Fig. 3) discloses an SOI substrate including a dielectric layer (22) including an air gap (30) at least partially beneath the active region (36). It would have been obvious for one skilled in the art at the time of the invention to use an air gap under the active region as disclosed by Delgado for the device of Gardner for the purpose, for example, of minimizing the parasitic capacitance between the upper and lower regions of the device (Delgado; column 3, lines 18-20 and 30-34).

In re claims 2-4, 25 and 26, Gardner in view of Delgado discloses the devices of claims 1, 20 and 24 respectively, wherein the trench contains a fill material consists of an air gap.

In re claims 5 and 21, Gardner in view of Delgado discloses the devices of claims 1 and 20 respectively, wherein the semiconductor layer includes silicon (Gardner; column 3, line 50).

1. Claims 6, 8, 9, 22, 27, 32 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnder in view of Delgado as applied to claims 1, 20 and 24, and further in view of Schwank et al. (U.S. Patent No. 6,268,630 B1).

In re claims 6, 22, 27, 32 and 37, Gardner in view of Delgado discloses the devices of claims 1, 20, 24 and 29 respectively, but does not expressly disclose the dielectric layer of the SOI substrate comprising silicon dioxide. However, silicon dioxide is a well-known insulator known to the prior art (Schwank; column 1, lines 56-57) and would have been an obvious choice for one skilled in the art to use in the SOI device of Gardner for the purposes of providing an SOI substrate.

In re claim 9, Gardner in view of Delgado discloses the device of claim 1, wherein the isolation region extends below the active layers into the bulk substrate (12), but does not expressly disclose the location of the buried SOI layer. Buried SOI layers, as shown by Schwank, are generally placed just under the active region. With this standard placement of the buried insulator SOI layer, the dielectric layer will include the air gap (claim 7), the trench will extend to a level of the dielectric layer of the substrate (claim 8), and the trench will extend at least partially into a level of the dielectric layer of the substrate (claim 9).

2. Claims 10, 13, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (as above) in view of Delgado and further in view of Chiang et al. (U.S. Patent No. 6,037,249).

In re claim 10, Gardner discloses a semiconductor device, comprising:

A substrate (12) including:

A dielectric layer (SOI substrate ; column 3, lines 50-51)

A semiconductor layer formed over the substrate;

A first active region (22) formed in the semiconductor layer;

A second active region (24) formed in the semiconductor layer; and

A trench (26) formed in the substrate and interposed between the first active region and the second active region.

Gardner does not expressly disclose the SOI substrate including an air gap for location at least partially beneath the active region. Delgado (esp. Fig. 3) discloses an SOI substrate including a dielectric layer (22) including an air gap (30) at least partially beneath the active

region (36). It would have been obvious for one skilled in the art at the time of the invention to use an air gap under the active region as disclosed by Delgado for the device of Gardner for the purpose, for example, of minimizing the parasitic capacitance between the upper and lower regions of the device (Delgado; column 3, lines 18-20 and 30-34).

Gardner does not expressly disclose the trench filled with a foamed polymeric material. Chiang (Fig. 5) discloses an isolation trench filled with a foamed polymeric material (106; column 3, lines 51-52), further comprising an air gap (107). It would have been obvious for one skilled in the art at the time of the invention to use the foamed polymer with air gap of Chiang for the device of Gardner for the purpose, for example, of further decreasing the capacitance between left and right active regions (Gardner, column 8, lines 33-36; Chiang, column 3, line 46).

In re claim 13, Gardner in view of Delgado and further in view of Chiang discloses the device of claim 10, wherein the semiconductor layer comprises a silicon layer.

In re claim 16, Gardner discloses a semiconductor device, comprising:

A substrate (12) including:

A dielectric layer (SOI substrate ; column 3, lines 50-51)

A semiconductor layer formed over the substrate;

A first active region (22) formed in the semiconductor layer;

A second active region (24) formed in the semiconductor layer; and

A trench (26) formed in the substrate and interposed between the first active region and the second active region.

Gardner does not expressly disclose the SOI substrate including an air gap for location at least partially beneath the active region. Delgado (esp. Fig. 3) discloses an SOI substrate including a dielectric layer (22) including an air gap (30) at least partially beneath the active region (36). It would have been obvious for one skilled in the art at the time of the invention to use an air gap under the active region as disclosed by Delgado for the device of Gardner for the purpose, for example, of minimizing the parasitic capacitance between the upper and lower regions of the device (Delgado; column 3, lines 18-20 and 30-34).

Gardner does not expressly disclose the trench filled with a cured aerogel. Chiang (Fig. 5) discloses an isolation trench filled with a cured aerogel (106; column 3, lines 52-53), further comprising an air gap (107). It would have been obvious for one skilled in the art at the time of the invention to use the foamed polymer with air gap of Chiang for the device of Gardner for the purpose, for example, of decreasing the capacitance between left and right active regions (Chiang; column 3, line 46).

In re claim 17, Gardner in view of Delgado and further in view of Chiang discloses the device of claim 16, wherein the semiconductor layer comprises a silicon layer.

3. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner/Delgado/Chiang as applied to claim 10 above, and further in view of Beyer et al. (U.S. Patent No. 5,098,856).

In re claims 11 and 12, Gardner/Delgado/Chiang discloses the device of claim 10 but does not expressly disclose the polymeric material comprising a polyimide. Beyer disclose an isolation trench comprising a polyimide polymer. It would have been obvious for one skilled in

the art at the time of the invention to use a polyimide as disclosed by Beyer for the device of Gardner/Chiang for the purpose, for example, of providing a beneficial material to aid in the manufacture of the device by providing a material that may be removed from the isolation trench (Beyer, column 2, lines 22-32).

4. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner/Delgado/Chiang as applied to claim 10 above, and further in view of Schwank et al. (as above).

In re claims 14 and 18, Gardner/Delgado/Chiang discloses the devices of claims 10 and 16 respectively, but does not expressly disclose the dielectric layer of the SOI substrate comprising silicon dioxide. However, silicon dioxide is a well-known insulator known to the prior art (Schwank; column 1, lines 56-57) and would have been an obvious choice for one skilled in the art to use in the SOI device of Gardner for the purposes of providing an SOI substrate.

5. Claims 29-31 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (as above) in view of Delgado et al. (as above).

In re claims 29 and 34, Gardner discloses a semiconductor device, comprising:

A substrate (12) including:

A dielectric layer (SOI substrate ; column 3, lines 50-51)

A semiconductor layer formed over the substrate;

A first active region (22) formed in the semiconductor layer;

A second active region (24) formed in the semiconductor layer;

A trench (26) formed in the substrate and interposed between the first active region and the second active region; and

Wherein the trench contains cells of gaseous components within an air gap (column 6, lines 16-18).

Gardner neither expressly discloses a plurality of transistors nor the active regions being a part of a memory or computer system. However, transistor layouts are well known in the art to comprise thousands of active regions, separate blocks of which are connected to memory systems, control systems and the like. It would have been obvious for one skilled in the art at the time of the invention to connect the semiconductor device of Gardner into a computer system comprising an isolated memory scheme or for the purpose, for example, of using a device layout that desires an isolation structure that provides excellent electrical isolation and enables tighter packing density with low capacitance (Gardner; column 8, lines 30-35).

Gardner does not expressly disclose the SOI substrate including an air gap for location at least partially beneath the active region. Delgado (esp. Fig. 3) discloses an SOI substrate including a dielectric layer (22) including an air gap (30) at least partially beneath the active region (36). It would have been obvious for one skilled in the art at the time of the invention to use an air gap under the active region as disclosed by Delgado for the device of Gardner for the purpose, for example, of minimizing the parasitic capacitance between the upper and lower regions of the device (Delgado; column 3, lines 18-20 and 30-34).

In re claim 30, Gardner in view of Delgado discloses the device of claim 29, wherein the trench contains a fill material of an air gap.

In re claims 35 and 36, Garnder in view of Delgado discloses the device of claim 34, wherein the trench contains a fill material of an air gap.

6. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner in view of Delgado as applied to claim 29 above, and further in view of Chiang (as above).

In re claim 31, Gardner in view of Delgado discloses the device of claim 29, but does not expressly disclose the trench containing a foamed polymeric material. Chiang (Fig. 5) discloses an isolation trench filled with a foamed polymeric material (106; column 3, lines 51-52), further comprising an air gap (107). It would have been obvious for one skilled in the art at the time of the invention to use the foamed polymer with air gap of Chiang for the device of Gardner for the purpose, for example, of further decreasing the capacitance between left and right active regions (Gardner, column 8, lines 33-36; Chiang, column 3, line 46).

Response to Arguments

7. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment to claims 1, 10, 16, 20, 24, 29 and 34 necessitated the new ground(s) of rejection presented in this Office action. Note that the limitations of the canceled claims, while similar to the amendments in the independent claims, are not identical to the new limitations in the independent claims. Therefore, a new search was required. Accordingly,

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

GEORGE ECKERT
PRIMARY EXAMINER